

APM32F425xG_F427xG

Errata Sheet

Version: V 2.0

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1 Overview

This manual mainly describes the limitations of the APM32F425xG_F427xG series products during use. If you encounter the application scenarios described in this manual while using these products, follow the solutions provided in the manual. If no solution is provided, please avoid using the products in such scenarios.

2 Errata List

Table 1 Errata List

| Category | Overview | Product Version |
|---|--|-----------------|
| | | B1 |
| ADC | When the ADC clock is 60MHz and the sampling rate is 4MSPS, the measured values of ENOB and THD are lower than the nominal values. | √ |
| ADC | For chips in LQFP144 package, when the ADC clock is 60MHz and the sampling rate is 4MSPS, the least significant bit of the conversion result is unreliable when collecting static data with values above 2000. | √ |
| ADC | When the ADC clock is 60MHz and the sampling rate is 4MSPS, the conversion results of ADC channels IN1~15 are slightly lower than expected. | √ |
| Bootloader | When the external high-speed clock (HSE) is used as the clock source and the oscillator frequency is greater than 20MHz, DFU and CAN cannot operate stably. | √ |
| Wake-up in Standby Mode | Operations before entering Standby mode | √ |

Note: √ indicates the item is applicable. × indicates the item is not applicable.

3 ADC

3.1 When the ADC clock is 60MHz and the sampling rate is 4MSPS, the measured values of ENOB and THD are lower than the nominal values

Problem description

When the ADC clock is 60MHz and the sampling rate is 4MSPS, the ENOB and THD parameters are worse compared to those at a 30MHz clock.

Solution

For applications sensitive to ENOB and THD, it is recommended to:

- (1) Lower the ADC clock to 40MHz or 30MHz;
- (2) Reduce the sampling rate or increase the sampling period.

3.2 For chips in LQFP144 package, when the ADC clock is 60MHz and the sampling rate is 4MSPS, the least significant bit of the conversion result is unreliable when collecting static data with values above 2000

Problem description

For LQFP144 packaged chips, when the ADC clock is 60MHz and the sampling rate is 4MSPS, collecting static data with values above 2000 may result in a deviation of at least 1 LSB.

Solution

For applications requiring high acquisition accuracy, it is recommended to:

- (1) Lower the ADC clock to 40MHz or 30MHz;
- (2) Reduce the sampling rate or increase the sampling period.

3.3 When the ADC clock is 60MHz and the sampling rate is 4MSPS, the conversion results of ADC channels IN1~15 are slightly lower than expected

Problem description

When the ADC clock is 60MHz and the sampling rate is 4MSPS, the conversion results of ADC channels IN1~15 are approximately 1.5 LSB lower than expected.

Solution

For applications requiring high acquisition accuracy, it is recommended to:

- (1) Use other ADC channels;
- (2) Lower the ADC clock to 40MHz or 30MHz;
- (3) Reduce the sampling rate or increase the sampling period.

4 Bootloader

4.1 When using an external high-speed clock (HSE) as the clock source, DFU and CAN cannot operate stably if the oscillator frequency is greater than 20MHz

Problem description

When an oscillator with a frequency above 20MHz is used as the external high-speed clock (HSE) for the APM32F425xG_F427xG, and the chip's HSI frequency deviation is in the negative range, the Bootloader's DFU and CAN functions cannot be used. In this case, the user can only update firmware via the Bootloader using the USART and I2C interfaces.

Solution

To use the Bootloader's DFU and CAN functions, an HSE oscillator with a frequency of 16MHz or lower must be selected.

5 Wake-up in Standby Mode

Problem description

In Standby mode, the system supports multiple wake-up sources. These signals are combined (using a logical OR) before reaching the rising edge detector. When a valid edge is detected, a wake-up flag (WUEFLG) is generated. To ensure the MCU enter and stay in Standby mode, you must clear the WUEFLG flag first; otherwise, it will wake up immediately. Note that if any active wake-up source stays high while clearing the flag (setting the WUFLGCLR bit), the detector's input also stays high. As a result, it cannot detect new level changes, which masks future wake-up events and prevents the MCU from waking up properly.

Solution 1

To prevent this issue, follow these steps before entering Standby mode:

- (1) Disable all used wake-up sources.
- (2) Clear all related wake-up flags.
- (3) Reenable all used wake-up sources.

Solution 2

Keep only one wake-up source before entering Standby mode (for example, turn off the RTC alarm and leave only the PA0 WKUP function on).

6 Revision History

Table 2 Document Revision History

| Date | Version | Revision History |
|---------------|---------|---|
| November 2025 | 1.0 | <ul style="list-style-type: none"><li data-bbox="480 353 683 383">● Initial release |
| April 2026 | 2.0 | <ul style="list-style-type: none"><li data-bbox="480 400 1302 430">● Delete Chapter 2: Product Version and Silk Screen Printing Instructions<li data-bbox="480 441 991 470">● Add Chapter 5: Wake-up in Standby Mode |

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